CE-ATA Technical Errata

Errata ID	**Protocol 013**
Affected Spec Ver.	**Protocol 1.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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Description of the specification technical flaw (add space as needed)

In standard MMC, some hosts may pull the CMD line high actively two clocks after reception of the response to an MMC command.

For CE-ATA, the host pulling the CMD line high actively after the response will not work with the command completion signal. This erratum calls out specifically that the host shall not actively pull the CMD line high after the response for RW_MULTIPLE_BLOCK (CMD61) if nIEN=0 in the ATA Control register. This is consistent with the existing timing diagrams for the command completion signal, specifically Figure 10 and Figure 12.

Description of the correction

The third paragraph of section 2.2 shall be modified as shown:

The device shall only transmit a command completion signal to the host after a RW_MULTIPLE_BLOCK (CMD61) has been issued by the host and the device has returned the R1(b) response for that MMC command and interrupts are enabled (nIEN=0 in the ATA Control register). When nIEN=0 in the ATA Control register, the host shall not drive the CMD line (i.e. leave the CMD line in a high impedance state) after sending the RW_MULTIPLE_BLOCK (CMD61) until two clocks after the command completion signal is received or until the host transmits the command completion signal disable.

Disposition log

08/30/2005	Erratum captured
10/3/2005	Erratum ratified

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